

IN THE SPECIFICATION:

Please replace paragraph [0019] with the following paragraph:

The circuit shown in the example in Figure 1 includes a ring oscillator 10 and an inverter 14 comprising an P-type transistor 11, and a N-type transistor 12. The oscillator 10 is connected to a different power supply (V_{RO}) than the inverter V_{DD} . The ring oscillator 10 is capable of producing a signal of very high frequency, f , above 100 Mhz (shown in the waveform in Figure 1) with period " t ". The device under test "DUT" (e.g., the capacitance of the gate oxide in this example) is shown as capacitor 40. Transistor 11 is connected to V_{DD} , while transistor 12 is connected to V_{SS} and, V_{SS} and V_{DD} can be chosen ($V_{DD} > V_{SS}$) to limit the voltage range across the DUT 40 and thus, make the capacitance measurements at a specific DC bias voltage, which is usually required for complete characterization of the DUT. Furthermore $V_{DD} - V_{SS}$ should be less than the sum of the absolute values of the threshold voltages of the n-type and p-type FETs that make up the inverter.